In the Specification

Please amend paragraph [0006] as follows:

Turbo has become one of the most used and researched encoding and decoding methods, as its performance is close to the theoretical Shannon limit. Turbo codes have ~~has~~ been adopted as a Forward Error Correct (FEC) standard in the so-called Third Generation (3G) wireless communication. Most of the development focus has been on a Very Large Scale Integration (VLSI), or hardware, implementation of Turbo Codes. However, VLSI implementation lacks flexibility in the face of multiple standards (WCMDA, CMDA2000, TD-SCDMA), different code rates (1/2, 1/3, 1/4, 1/6) and different data rates (from several kilo bits/s to 2Mbits/s). Accordingly, different VLSI chips have to be designed toward different standards, code rates, data rates, etc. On the other hand, general-purpose processors or DSP processors cannot meet the requirements of high data rate and low power consumption for a mobile device.

Please amend paragraph [0009] as follows:

Figure 3 is a timing diagram of a sliding window ~~BCJR~~ Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm.

Please amend paragraph [0024] as follows:

A generic Turbo decoder is shown in Figure 2. The Turbo decoder contains two "soft" decision decoders (DEC1 and DEC2), associated with two RSC encoders, and an interleaver and de-interleaver between these two decoders as shown in Figure 2. The decoders generate "soft" outputs, which ~~refers~~ refer to the reliability of the outputs. Basically, there are two different algorithms for generating soft outputs. The first is called symbol-by-symbol MAP (Maximum *A Posteriori*). The second is known as Soft Output Viterbi Algorithm (SOVA). The details of MAP and SOVA, as well as a comparison of the two algorithms, are known to those with the requisite skill in the art, but beyond the scope of this description. The MAP algorithm essentially has better performance than the SOVA algorithm at the expense of a more complicated implementation. In accordance with the invention, MAP algorithm is preferably used for executing Turbo decoding on a reconfigurable SIMD processor array. However, this invention

can also accomplish Turbo decoding by mapping the SOVA algorithm to the processor array. A summary of the MAP algorithm follows.

Please amend paragraph [0063] as follows:

This parallel mapping is based on the MIX-LOG-MAP algorithm. The window size is twice the number of trellis states in each stage. Basically, the sliding window approach is suitable for the large frame size of CDMA2000, W-CDMA and TD-SCDMA. Parallel mapping has a higher performance, uses less memory, but has higher power consumption compared to serial mapping. The following tables show the steps for each kernel. They are ~~the~~ similar ~~as~~ to the steps in the serial mapping. The resource allocation for each computational procedure in the parallel mapping is shown in Figure 14.

Please amend the Abstract as follows:

A digital processing apparatus and method for executing a turbo coding routine. The apparatus and method includes adapting a turbo coding algorithm for execution by one or more reconfigurable processing elements from an array of processing elements, and ~~then~~ mapping the adapted algorithm onto the array for execution. A method includes configuring ~~a portion of~~ an array of independently reconfigurable processing elements for performing a turbo coding routine, and executing the turbo coding routine on data blocks received at the configured portion of the array of processing elements. An apparatus includes an array of interconnected, reconfigurable processing elements, where each processing element is independently programmable with a context instruction. The apparatus further includes a context memory for storing and providing the context instruction to the processing elements, and a processor for controlling the loading of the context instruction to the processing elements~~, for~~ while configuring ~~a portion~~ the processing elements to perform the turbo coding routine.